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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/692,938

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02/03/2006

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EXAMINER

TRINH, HOA B

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 02/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/692,938

Applicant(s)

SUGAYA ET AL.

Examiner

Vikki H. Trinh

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Applicant's amendment filed on 11/16/05 has been considered. Claims 2-3, and 15-35 have been canceled. Claims 1, and 4-14 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, and 4-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohuchi (6,590,287) in view of Yamaguchi et al. (6,930,388) (hereinafter Yamaguchi).

Ohuchi discloses a semiconductor device having a semiconductor element 6 (fig. 6d) , an electrode part 8 (fig. 6d), a wiring substrate 1 (fig. 6d), having an insulation layer 3, 4 (fig. 6d), an electrode-part-connection electrode 2, 5 (figs. 3e, 6d), an external electrode 7 (fig. 6d) that is connected electrically with the electrode –part-connection electrode 5, and the electrode part 8 and the electrode-part-connection electrode 2, 5 (fig. 6d) being connected electrically with each other by a metal joint 5 (fig. 3e, col. 6, lines 40-43). Note that Ohuchi teaches that layers 5 have more than one layer (col. 9, line 1). Furthermore, Ohuchi discloses the electrode part 8 (fig. 6d) and the connection electrode 2, 5 (fig. 3e and fig. 6d) include metal layers made of at least one of metal selected from the group consisting of noble metals and solder alloys (col. 6, lines 48-55, col. 8, lines 60-65, col. 15, line 35), and the metal layer of the electrode part 8 and the metal layer of the electrode part connection electrode 2, 5 are connected by the metal joint 5 (fig. 3e). Moreover, Ohuchi discloses the semiconductor element 6 (fig. 6d) includes a plurality of the electrode parts 8,5,2,7 and a surface of the wiring substrate 1 and the surface of the semiconductor element 6 are bonded with each other so that spaces between the electrode parts are filled with the insulation layer 3, 4 (fig. 3e and fig. 6d).

However, Ohuchi does not explicitly teach that the insulation layer has an elastic modulus' range between .1Gpa to 5Gpa.

Yamaguchi teaches an analogous semiconductor device having a substrate 9 and an insulation layer 5 having an elastic modulus' range of .1GPa to 10 GPa (col. 7, lines 12-13).

Therefore, as to claim 1, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Ohuchi with the insulation having the elastic modulus' range, as taught by Yamaguchi, so as to provide an alternative insulation material for the device.

As to claim 4 Ohuchi shows that a surface of the wiring substrate crossing is larger than a surface of the semiconductor element crossing (fig. 1a).

As to claim 5, Ohuchi shows that the external electrode 7 (fig. 6d) is arranged on a surface of the insulation layer 3 that is seen when the semiconductor device is observed in the thickness direction thereof from a semiconductor element side, as broadly interpreted.

As to claim 6, Ohuchi teaches that the wiring substrate 1 (fig. 1b) further includes an inner via (fig. 1b) that is provided in the insulation layer 3 (fig. 1b) so as to go through the insulation layer 3 in a thickness direction thereof, and the electrode-part-connection electrode 2, 5 (fig. 1b) and the external electrode 7 (fig. 1b) are connected electrically through the inner via (fig. 1b).

As to claim 7, Ohuchi teaches that the wiring substrate 1 (fig. 1b) further includes at least one wiring layer 7 (fig. 1b) arranged in the insulation layer 3 fig. 1b).

As to claim 8, Ohuchi discloses the insulation layer 3 or 4 (fig. 1b) is made of a material containing a thermosetting resin (see Table 1, col. 10).

As to claim 9, Ohuchi discloses the range for the claim's limitations such that the range includes the material containing a thermosetting resin with about 75 wt% to 91 wt% of an

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inorganic filler, and about 9 wt% to 25 wt% of a resin composition containing a thermosetting resin (See Table 1, col. 10).

As to claim 10, Ohuchi discloses that the thermosetting resin contains at least one kind of resin selected from the group consisting of epoxy resins (See Table 1, col. 10).

As to claim 11, Ohuchi teaches in the case where the material containing the thermosetting resin does not contain thermosetting polyimide, the material containing the thermosetting resin contains a thermosetting resin with a glass transition temperature of not lighter than 150°C (See Table 1, col. 10).

As to claim 12, Ohuchi and Yamaguchi disclose the invention substantially as claimed. However, Ohuchi and Yamaguchi do not teach a range of thickness for the semiconductor element as claimed in the present invention. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Ohuchi and Yamaguchi with a range of thickness for the semiconductor element as claimed, since it is a prima facie obvious to an artisan for routine experimentation and optimization in selecting a specific range of thickness because applicants have not yet established any criticality for the specific range.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

As to claim 13, Ohuchi discloses that the thickness of the insulation layers (layer 3 thickness plus layer 4 thickness) (fig. 1b) is within (col. 7, lines 6-26) the claimed range.

As to claim 14, Ohuchi and Yamaguchi disclose the invention substantially as claimed. However, Ohuchi and Yamaguchi do not teach a range of thickness for the semiconductor device as claimed in the present invention. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Ohuchi and Yamaguchi with a range of thickness for the semiconductor device as claimed, since it is a prima facie obvious to an artisan for routine experimentation and optimization in selecting a specific range of thickness because applicants have not yet established any criticality for the specific range.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)

Response to Arguments

5. Applicant's arguments filed 11/16/05 have been fully considered but they are not persuasive.

In the remarks, applicants argue that the rejection above with respect to the critical nature of the range dimensions in the present application claims. Specifically, applicants state that "the specification clearly discloses [the critical nature] that even if the electrode part and the electrode part connection electrode are connected directly by a metal joint, rather than a bump, the wiring

substrate including the insulation layer with an elastic modulus of the claimed range enables the reduction of stresses occurring due to the thermal expansion difference between the semiconductor element and the wiring substrate". This statement does not overcome the critical factor in the rejection. As stated in the rejection, Ohuchi discloses all of the elements as claimed, except claimed dimensions for the semiconductor device. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Ohuchi and Yamaguchi with a range of thickness for the semiconductor device as claimed, since it is a prima facie obvious to an artisan for routine experimentation and optimization in selecting a specific range of thickness because applicants have not yet established any criticality for the specific range. Note that Ohuchi lacks the insulation layer with the specific range of modulus. Yamuguchi cures the deficiency in Ohuchi by disclosing the insulation with the range of modulus as claimed. Note also that Ohuchi and Yamaguchi disclose analogous semiconductor device.

For the foregoing reasons, the rejection is maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

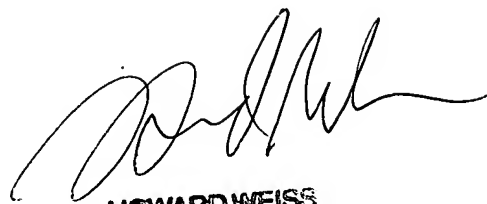
Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests

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to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,
Patent Examiner
AU 2814



HOWARD WEISS
PRIMARY EXAMINER